## 450W, 50V High Power RF LDMOS FETs

### Description

The YC1245V is a 450-watt, high performance, internally matched LDMOS FET,

designed for avionics applications with frequencies 960 to 1215MHz.

It is featured for high power and high ruggedness.

### It is recommended to use this device under pulse condition only

 Typical Performance (on Yingtron wide band test fixture with device soldered): Pulse width:100uS, duty cycle: 10%, TA = 25 °C

Vds	=	50	V,	ldq	=	230	mA

Freq(MHz)	Pin(dBm)	P2.5dB(dBm)	P2.5dB(W)	IDS(A)	Gain(dB)	Eff(%)
960	41.8	56.82	480	2.11	15.02	50.5
990	41	57.44	554	2.37	16.44	51.2
1030	42.1	57.65	582	2.39	15.55	53.3
1090	41.7	57.83	606	2.32	16.13	57.3
1160	41.1	57.35	543	2.01	16.25	60.2
1200	40.7	56.8	478	1.78	16.1	60.7
1215	41.1	56.72	469	1.75	15.62	60.8

#### Vds = 55 V, Idq = 230 mA

Freq(MHz)	Pin(dBm)	P3dB(dBm)	P3dB(W)	IDS(A)	Gain(dB)	Eff(%)
960	42.5	57.4	550	2.22	14.9	49.9
990	41.9	58.13	650	2.58	16.23	50.0
1030	43	58.3	676	2.6	15.3	51.6
1090	42.7	58.43	697	2.56	15.73	54.0
1160	42	58.06	640	2.25	16.06	57.2
1215	42.1	57.5	562	1.98	15.4	58

### Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

#### Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
DrainSource Voltage	V <sub>DSS</sub>	115	Vdc
GateSource Voltage	V <sub>GS</sub>	-10 to +10	Vdc



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Operating Voltage		V <sub>DD</sub>	+55			Vdc	
Storage Temperature Range		Tstg	-65 to +150			°C	
Case Operating Temperature		T <sub>c</sub>		+150		°C	
Operating Junction Temperature		TJ		+225		°C	
Table 2. Thermal Characteristics	1	<b>I</b>					
Characteristic	Sy	/mbol		Value		Unit	
Thermal Resistance, Junction to Case, Case Temperature							
80°C, 600W Pout, Pulse width: 100us, duty cycle: 10%,	F	Rejc		0.03		°C/W	
Vds=50 V, IDQ = 230 mA, frequeny:1090MHz							
Table 3. ESD Protection Characteristics							
Test Methodology				Class			
Human Body Model (per JESD22A114)		Class 2					
Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)							
Characteristic		Symbol	Min	Тур	Max	Unit	
DC Characteristics							
Drain-Source Breakdown Voltage			445				
(V <sub>GS</sub> =0V; I <sub>D</sub> =100uA)		V <sub>DSS</sub>	115			V	
Zero Gate Voltage Drain Leakage Current					10		
$(V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V})$		I <sub>DSS</sub>			10	μΑ	
GateSource Leakage Current					1		
$(V_{GS} = 6 V, V_{DS} = 0 V)$		I <sub>GSS</sub>			I	μΑ	
Gate Threshold Voltage		V <sub>GS</sub> (th)		1.0			
$(V_{DS} = 50V, I_{D} = 600 \text{ uA})$				1.0		v	
Gate Quiescent Voltage		V		2.77		V	
( $V_{DD}$ = 50 V, $I_{DQ}$ = 230 mA, Measured in Functional Test)	$(V_{DD} = 50 \text{ V}, I_{DQ} = 230 \text{ mA}, \text{Measured in Functional Test})$			2.11		V	

Functional Tests (In Yingtron test fixture, 50 ohm system) : V<sub>DD</sub> = 50 Vdc, I<sub>DQ</sub> = 230 mA, f = 1090MHz, Pulse CW Signal Measurements. (Pulse

Width=100 µs, Duty cycle=10%), Pin=42dBm

Power Gain @ Pout	Gp		16	dB
Output Power	Pout	500	600	W
Drain Efficiency@Pout	$\eta_{\text{D}}$		57	%
Input Return Loss	IRL		-5	dB

## Reference Circuit of Test Fixture Assembly Diagram (Layout file upon request)

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Figure 1. Test Circuit Component Layout

## Table 5. Test Circuit Component Designations and Values(Layout file upon request)

Part	Description	model	
C1~C5	33PF	ATC800B	
C6	1.8PF	ATC800B	
C7,C8	4.7PF	ATC800B	
C9,C10	5.1PF	ATC800B	
C11~C14	2.2PF	ATC800B	
C15,C16	1.2PF	ATC800B	
C17,C18	0.5PF	ATC800B	
C19,C20,C21	10UF	100V/10UF	
C22,C23	2200UF	63V/2200UF	
R1	10Ω	0805	
Q1	YC1245V	183608S-01	
PCB	4350B	30Mil	

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## **TYPICAL CHARACTERISTICS**

Pulse width:100uS, duty cycle: 10%, Vds = 50 V, Idq = 230 mA, TA = 25 °C at fixed Pin=46.5dBm

Figure 2: Efficiency as a Function of output power



Figure 3: Power gain as a Function of output power



Figure 3: Network analyzer plot (S11 and S21)



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## **Package Outline**



OUTLINE	REFERENCE			EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	
PKG-Z2E					09/19/2018

## **Revision history**

#### Table 6. Document revision history

Date	Revision	Datasheet Status
2018/9/19	Rev 1.0	Preliminary Datasheet Creation

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